Amendments to the Specification

Please *amend* the carryover paragraph of pages 8 to 9 as follows:

Returning now to Fig. 1B, one phase portion of the receive stream is processed or qualified through flip-flop 158 on the falling edge of the clock. The remainder (e.g., the other phase) passes directly to XOR 162. The XOR gates thus compare the test signals (i.e., the stimuli) to the response produced by DDR multiplexer 120. In particular, XOR gate 160 compares the output of flip-flop 108 (or, alternatively, the data fed to flip-flop 108) with the corresponding portion of the DDR output produced by DDR multiplexer 120, while XOR gate 162 ~~160~~ compares the output of flip-flop 104 (or, alternatively, the data fed to flip-flop 104) with the corresponding portion of the DDR output.

_____If the transmission circuitry of the I/O interface is operating correctly, the evaluation logic (e.g., XOR gates 160, 162) should remain low. Otherwise, if an error is detected, OR gates 164, 166 carry a high signal to result flip-flop 170, which raises bistFlag 172 to indicate an error and feeds this signal back to OR gate 166 to retain the error. It may be seen that macro cell 100 evaluates the DDR output in real-time, as it is fed to the evaluation logic of Fig. 1B. More specifically, the DDR output is not stored for later comparison.